SUBCONTRACT TITLE: ***ADVANCED PROCESSING OF CdTe- AND $CuIn_XGa_{1-X}Se_2$-BASED SOLAR CELLS***

SUBCONTRACT NO: **NDJ-2-30630-18**

REPORT FOR: Phase III/Quarter 2

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This is the progress report for the 2nd quarter of Phase III of the above subcontract. The project deals with two thin film technologies: CdTe and CIGS. The focus areas include: (a) CdTe – stability, novel back/front contacts, and the development of manufacturing friendly processes; (b) CIGS – development of two-step non-co-evaporation technology.

Part I – CdTe

Front Contact Studies

The effectiveness of bi-layer front contacts in CdTe has been demonstrated by several groups, including the CdTe Group at NREL that has achieved the current record efficiency of 16.5% using zinc stannate (ZTO) as the high resistivity (high-ρ, or buffer) layer in their CdTe devices; zinc stannate refers to two types of oxides depending on the film stoichiometry: (a) Zn_2SnO_4 has a cubic spinel structure, and (b) $ZnSnO_3$ has an orthorhombic structure. In this report we discuss the material properties and device characteristics of Zn-Sn-O based films and solar cells. The Zn-Sn-O films are being deposited by co-sputtering from ZnO and SnO_2 targets (4N), a process that allows variation and control of film stoichiometry. Our main focus for this work has been to study the effect of film stoichiometry (i.e. Zn/Sn ratio); the term "Zn/Sn ratio" refers to the as-deposited film ratio determined through calibration runs using EDS; to-date the Zn/Sn ratio was varied from 1.5 to 3.0, with most experiments focusing on the ratio of 2.0 (in order to obtain the Zn_2SnO_4 phase of zinc stannate). In nearly all instances the Zn-Sn-O films were heat treated; the final Zn/Sn ratio i.e. in the annealed films was not measured (this will be addressed in future work). In order to maintain control of the Zn/Sn ratio, the process was recalibrated every 4-5 depositions, and every time a substantial change in the Zn/Sn ratio was made. In addition to the effect of the Zn/Sn ratio, the effect of the deposition and annealing temperatures of the Zn-SnO films was also studied. Since the main effect of Zn-Sn-O films is that they allow the use of thinner CdS, the thickness of the CdS was also varied; this was done primarily by adjusting the conditions of the $CdCl_2$ heat treatment (i.e. temperature) to promote the consumption of CdS. Additional information on the Zn-Sn-O process has been included in previous reports. Solar cells were fabricated using "baseline" procedures: these include CBD CdS, CSS CdTe, and doped graphite contact; the device structure was:
SnO_2:F/Zn-Sn-O/CdS(CBD)/CdTe(CSS)/graphite-HgTe:Cu.

Structural Properties of Zn-Sn-O Films

The XRD spectra for as-deposited and annealed Zn-Sn-O films are shown in Fig. 1. The Zn/Sn ratio for these was 2.0 (in as-deposited films); all films shown were deposited at room temperature on SnO_2:F coated glass substrates; therefore, if the SnO_2 phase forms within the Zn-Sn-O film it will not be possible to detect. Data for the SnO_2/glass substrate are also included (top plot) as a reference; the SnO_2 peaks are located at 26.63, 51.80, and 54.78°. The as-deposited Zn-Sn-O films appear to be amorphous, and begin to crystallize at a 575°C; the dotted line marks the location of the (311) plane of Zn_2SnO_4 (@ approx. 34.30°). Although higher annealing temperatures were also utilized, the films cracked and peeled off on several occasions; therefore for subsequent experiments the annealing temperatures were limited to a maximum of 600°C.

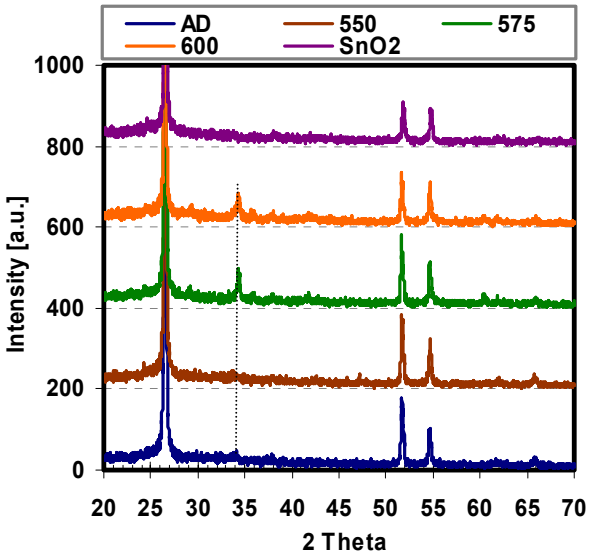

Figure 1. XRD spectra for as-deposited and annealed Zn-Sn-O films

The co-deposition process offers the option to vary the film stoichiometry. A series of films were deposited at different Zn/Sn ratios (1.5-2.5). Figure 2 shows the XRD spectra of Zn-Sn-O films deposited over this range (all films have been heat treated in inert ambient at 600°C). Table 1 lists the various planes (and phases) identified from these data; as indicated above, since these films are deposited on SnO_2 it is not possible to determine whether SnO_2 has formed within the Zn-Sn-O films. In summary the results shown in Fig. 2 suggest that:

- For Zn-rich and near stoichiometric films (Zn/Sn=1.9-2.5) the Zn_2SnO_4 phase dominates

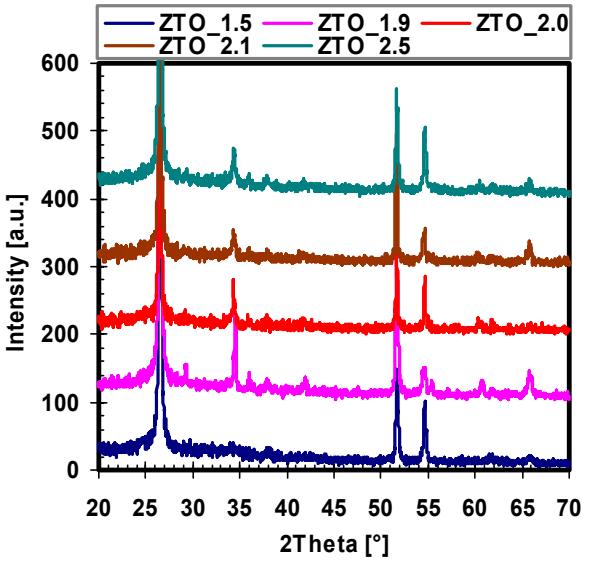

Figure 2. XRD spectra for Zn-Sn-O films deposited at different Zn/Sn ratios; annealed at 600°C

Table 1. XRD peaks identified for the films shown in Fig. 2

Zn/Sn	Zn_2SnO_4	$ZnSnO_3$
1.5	None	(006)
1.9	(220), (311), (222), (400), (440)	(006)
2.0	(311), (222), (400), (440)	(006)
2.1	(311), (222)	None
2.5	(311), (222)	(006)

- For Zn-poor films, the Zn_2SnO_4 phase is not detected; only small reflections from the $ZnSnO_3$ are found
- In most films both zinc stannate phases (Zn_2SnO_4 and $ZnSnO_3$) are found to be present

Another process parameter considered is the substrate temperature. The two films shown in Fig. 3 were deposited with a Zn/Sn ratio of 2.0 at a substrate temperature of 400ºC; one of these was subsequently heat treated at 600ºC. A key difference between these Zn-Sn-O films and the ones discussed above (all of which were deposited at room temperature) is the relatively low intensity of the Zn_2SnO_4 peaks. Instead, the highest intensity peaks (excluding those from the SnO_2 substrate) correspond to the $ZnSnO_3$ and ZnO_2 phases. This is the only case (i.e. high deposition temperature) where a binary oxide phase was identified. Table 2 summarizes the results of the XRD measurements.

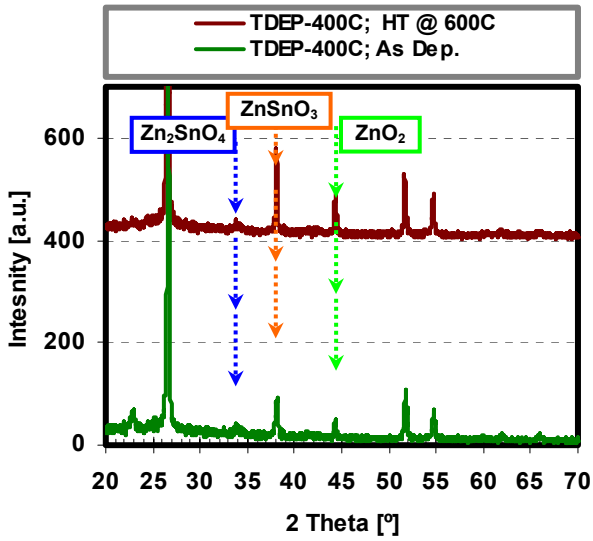

Figure 3. XRD spectra for Zn-Sn-O films deposited at 400ºC

Table 2. List of peaks identified in the Zn-Sn-O films shown in Fig. 3 (deposited at T_{SUB}=400°C)

	Zn_2SnO_4	$ZnSnO_3$	ZnO_2
AD.	(311)	(006)	(211)
AD/HT @ 600C	(311)	(012), (006)	(211)

Resistivity

The resistivity of the Zn-Sn-O films was measured using the 4-point probe method. The results of these measurements are summarized in Fig. 4; all films shown were deposited at room temperature and annealed in inert ambient; the resistivity of as-deposited films was in most cases too high to measure with the 4-point probe method (and is not shown in this figure).

In summary the results in Fig. 4 suggest the following:

- Although the resistivity of films annealed at 550°C is lower than that of the as-deposited films, it is still the highest in this set of samples; this could be due to their structural properties. Since as indicated previously (Fig. 1) films annealed at 550°C remained amorphous their mobility may be too low affecting their resistivity.
- In general the resistivity decreases with increasing annealing temperature; again this could be due to improvements in crystallinity as indicated by the XRD measurements in Fig 1.
- The resistivity increases with Zn content; the reason for this is not clear at this time, and based on the limited measurements it is not possible to speculate on the role of the various phases identified with XRD.

One exception to the trends observed in Fig. 4 is the film deposited with a Zn/Sn ratio of 1.0 and annealed at 550°C; this film has the lowest resistivity (this result will be verified in the future). It should be mentioned that the films deposited on glass (used for resistivity measurements) may not crystallize to the same extent as the films shown in Figs 1-3, that were deposited on SnO_2 substrates. This issue will also be addressed in future experiments (i.e. structural differences due to substrate effects).

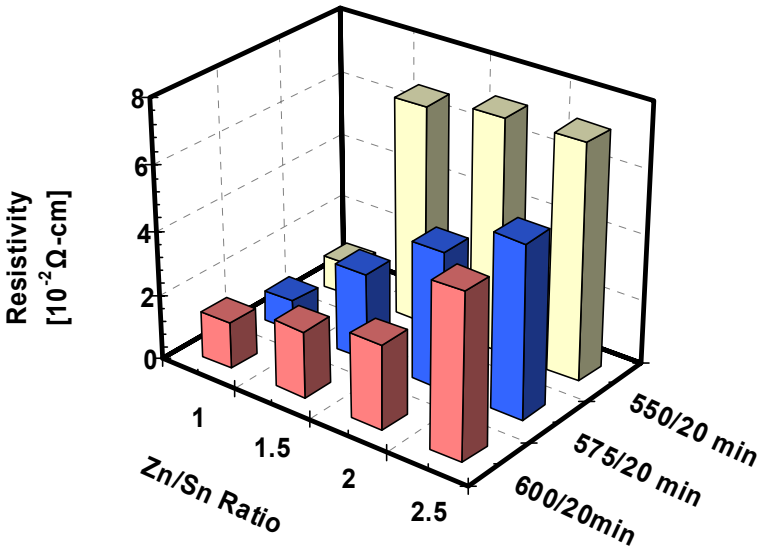

Figure 4. The resistivity of Zn-Sn-O films as a function of the Zn/Sn ratio and annealing conditions

Zn-Sn-O-Based Solar Cells

Solar cells were fabricated on glass/SnO_2:F/Zn-Sn-O substrates following baseline procedures i.e. CBD CdS, CSS CdTe, $CdCl_2$ HT, doped graphite back contact. Most Zn-Sn-O films used for cells to be discussed below, originated from the same deposition runs as the films shown in Figs 1-3.

Effect of Zn-Sn-O Annealing Temperature

The SR, dark J-V, and solar cell characteristics for CdTe solar cells fabricated with as-deposited and annealed Zn-Sn-O films are shown in Figs 5 and 6 and table 3. The blue response of these cells suggests that the CdS films in the completed devices are thinner for cells fabricated with as-deposited and annealed at 550°C Zn-Sn-O films; all devices shown were fabricated with CdS of the same starting thickness (same deposition run) and received the same $CdCl_2$ HT. Therefore, the reason for the loss in CdS is believed to be the fact that the Zn-Sn-O films in these two cells were amorphous, and intermixed to a greater extent than the films annealed at 575 and 600°C, which as indicated in a previous section became polycrystalline. The dark J-V characteristics of these devices clearly show that the dark currents (J_O) for the devices with amorphous Zn-Sn-O are higher. The device with Zn-Sn-O annealed at 575°C exhibits some dark shunting, not present in the cell fabricated with Zn-Sn-O annealed at the highest temperature of 600°C. The solar cell characteristics for these four cells, listed in table 3, clearly show the improved performance of the devices with Zn-Sn-O annealed at the two highest temperatures. These results clearly demonstrate the effect of the structural properties of Zn-Sn-

O films on solar cell performance: it is necessary that the films are polycrystalline for optimum performance. However, these devices also exhibit loss in performance with thinner CdS, suggesting that Zn-Sn-O does not offer an advantage over other "buffers" for devices with thin CdS. The improvement in performance with the Zn-Sn-O annealing temperature was also discussed in a previous report. Based on these results the annealing temperature for Zn-Sn-O films was fixed at 600°C for cell fabrication. The decrease in the series resistance (R_S) with increasing annealing temperature could be related to the resistivity of Zn-Sn-O films, that as discussed above it decreases with annealing temperature and improved film crystallinity.

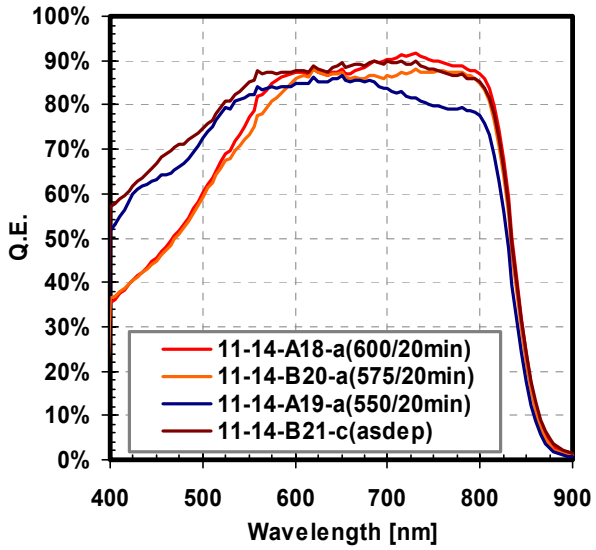

Figure 5. SR of cells fabricated on as-deposited and annealed Zn-Sn-O films (Zn/Sn=2.0)

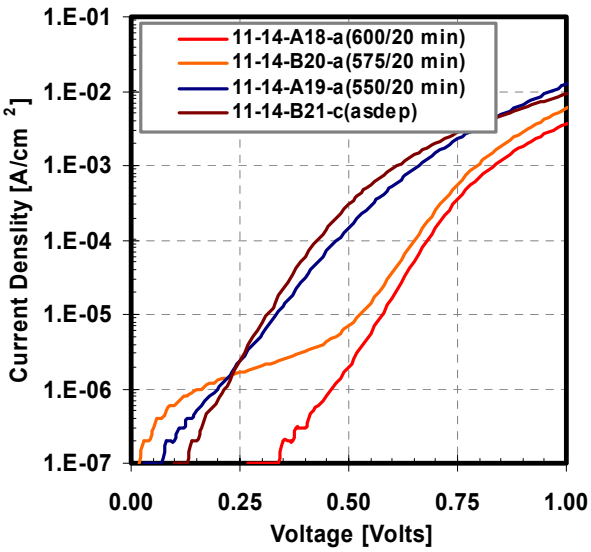

Figure 6. Dark Ln(J)-V for the cells shown in Fig. 5

Table 3. Solar cell performance characteristics for the cells shown in Figs 5 & 6

Zn-Sn-O	V_{OC} [mV]	FF [%]	J_{SC} [mA/cm^2]	R_S (L) [Ω-cm^2]	R_{SH} (L) [Ω-cm^2]
AD	730	58.0	23.40	2.05	1100
HT 550 ºC	730	55.0	22.00	2.10	1000
HT 575 ºC	820	68.0	21.40	1.55	1170
HT 600 ºC	830	69.0	22.00	0.96	900

Effect of Zn/Sn Ratio

The effect of the Zn/Sn ration in Zn-Sn-O films was studied by depositing the films at ratios from 1.5 to 2.5 and subsequently annealing them at 600°C. The characteristics of these cells are summarized in Figs 7 and 8 and table 4. All CdS films had the same initial thickness and all cells were exposed to the same $CdCl_2$ heat treatment, therefore, the only remaining difference that could influence the CdS thickness is the Zn-Sn-O buffer. The blue response suggests that the cells for which the Zn/Sn ratios were 2.1 and 2.5 (i.e. excess Zn) end up with the thickest CdS (after completing the cell fabrication process); the cells with Zn/Sn ratios below 2.0 show an increased blue response, therefore thinner CdS. These results seem to suggest that CdS consumption also depends on the Zn-content (i.e. composition) of the Zn-Sn-O films in addition to their structural characteristics (amorphous vs. polycrystalline) as discussed in the previous

section. As noted for the cells discussed in the previous section, solar cell performance continues to degrade with decreasing CdS thickness, with the FF decreasing to a greater extent than V_{OC} as shown in table 4. The dark J-V for these devices do not offer a clear correlation with device performance, primarily due to the fact that dark shunting and series resistance effects seem to dominate some of some devices; nevertheless, the best device (Zn/Sn=2.5) does exhibit the lowest dark current.

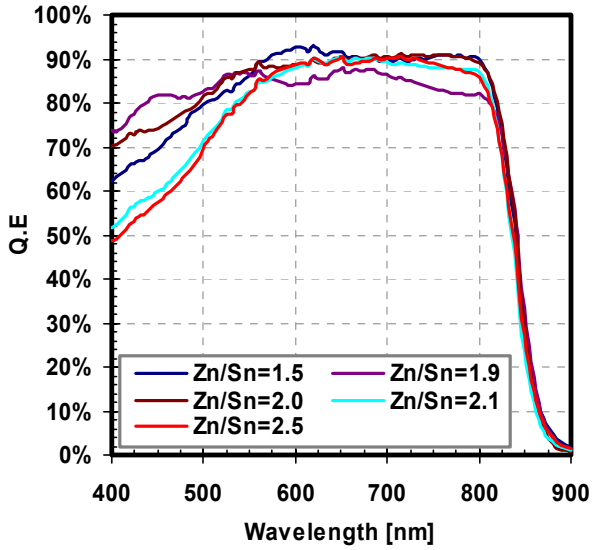

Figure 7. SR of cells fabricated with Zn-Sn-O films deposited with different Zn/Sn ratios - annealed at 600°C

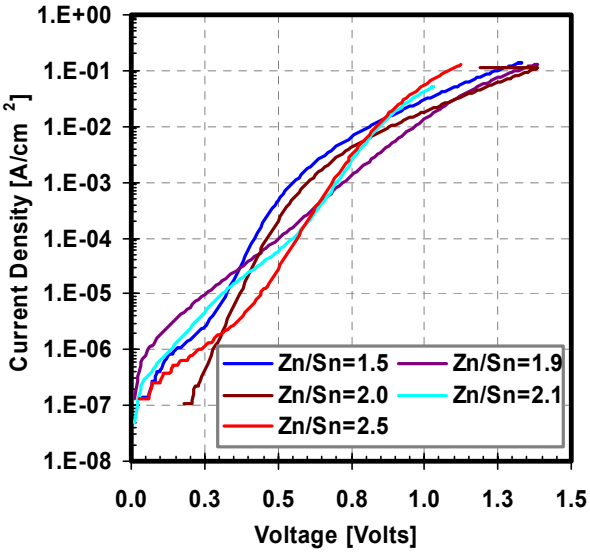

Figure 8. Dark Ln(J)-V characteristics of the cells shown in Fig. 7

Table 4. Solar cell performance characteristics for the cells shown in Figs 7 & 8

Zn/Sn Ratio	V_{OC} [mV]	FF [%]	J_{SC} [mA/cm^2]	R_S [Ω-cm^2]	R_{SH} [Ω-cm^2]
1.5	710	54.6	24.40	2.32	500
1.9	770	44.3	24.00	2.34	730
2.0	780	58.2	24.50	2.30	800
2.1	810	66.6	23.10	2.50	800
2.5	790	66.7	23.00	1.40	900

Effect of Zn-Sn-O Deposition Temperature

As discussed in a previous section, Zn-Sn-O films deposited at higher substrate temperatures (400°C; Zn/Sn=2.0) were found to contain ZnO_2 in addition to the zinc stannate phases. Several such Zn-Sn-O films with different thickness were used for cell fabrication. Spectral response data and device performance are summarized in Figs. 9 and 10, and table 5. Clearly in all cases the blue response is relatively high (i.e. thin CdS) to the extent that solar cell performance should degrade. However, as indicated in table 5 all devices exhibit high V_{OC}s and FFs; these cells also exhibit the highest shunt resistances of all the cells discussed in this report, suggesting that the buffer properties (and in general the CdS/buffer interface) are critical to improving this device parameter (R_{SH}). Subtle differences in the SRs shown in Figs 9 and 10 could be related to the duration of the Zn-Sn-O annealing, which as indicated in the figures was carried out for 5 and 20 minutes respectively; this effect will be further studied in future work. It is therefore concluded that the composition of the Zn-Sn-O films is key to achieving optimum

performance at small CdS thicknesses; the $ZnSnO_3$ phase dominated the XRD spectra of the Zn-Sn-O (deposited at T_{SUB}=400°C), in addition to the presence of ZnO_2. This work will continue in order to verify some of the results discussed in this report as well as further explore the effect of Zn-Sn-O films on solar cell performance.

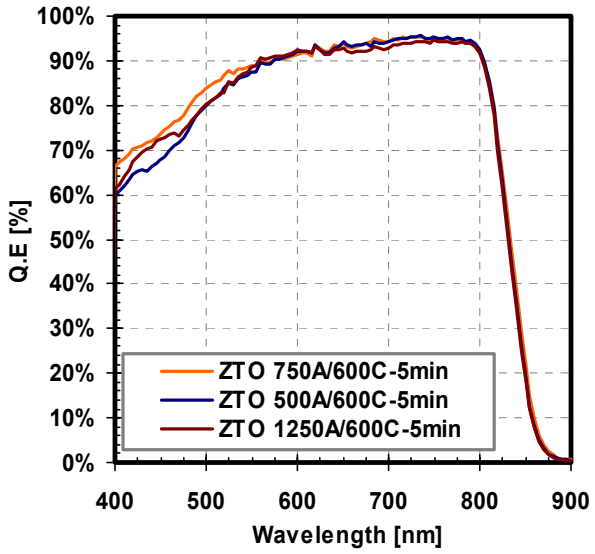

Figure 9. SR of cells fabricated with Zn-Sn-O films deposited at 400° - annealed at 600° for 5 mins

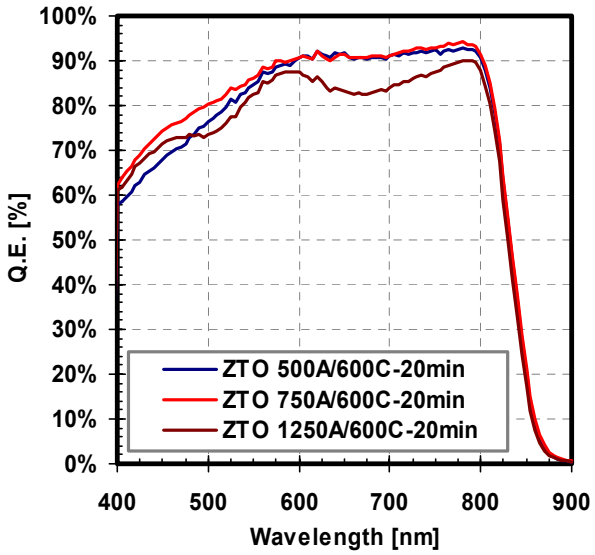

Figure 10. SR of cells fabricated with Zn-Sn-O films deposited at 400° - annealed at 600° for 5 mins

Table 5. Solar cell performance characteristics for cells fabricated with Zn-Sn-O films deposited at 400°C

Zn-Sn-O Thickness. [Å]	V_{OC} [mV]	FF [%]	J_{SC} [mA/cm^2]	R_S [Ω-cm^2]	R_{SH} [Ω-cm^2]
500	840	68.2	24.40	1.64	1700
500	830	71.0	23.80	1.44	1700
500	830	69.3	24.74	1.33	1900
750	830	68.2	24.84	1.75	1900
1250	820	69.1	24.39	1.47	2000

Part II - CIGS

Annealing Studies

Background

We are in the process of reducing the thickness of our devices to reduce processing time and materials utilization. Because of the complexity of our time/temperature profile during deposition when the thickness is reduced by decreasing deposition time, the time at temperature is also altered. It is necessary to understand what role this plays in film formation and performance. Also, it is important to understand whether post deposition annealing has a role to play in making up for the lowered thermal exposure during growth. To this end we have conducted a series of experiments to determine the effect of annealing on device performance. It is commonly reported in the literature that some type of anneal is used to improve device performance. Light soaking is also commonly used before making characterization measurements. While we have observed improvement in our devices with light soaking, annealing has not produced the results claimed by others. Clearly this is due to the different nature of our devices which are deposited by two-step all-solid-state processing. A noteworthy difference for our devices is that we deposit a thin (~ 25 Á) layer of Cu at the end of our deposition. This is not done by others, and it is likely that this step affects the top interface region in subtle ways that might lead to different behavior upon annealing. The Cu top layer is deposited at about 450°C and the substrate temperature is subsequently raised to 550°C. It is likely that the Cu has moved to wherever it can and has bonded. The total Cu/Group III ratio in our films is still below one.

Experimental

Details of our device process have been reported in previous reports and papers. The main experimental detail for this study is the annealing procedure. In all cases, unless indicated otherwise, the samples were annealed in vacuum at 250°C for 2 minutes. Overall the ramp–up time to temperature was about 10 minutes, and the cool-down time was about 30 minutes.

Results and Discussion

In Fig. 11 we show the V_{OC} profile for our reference run. This is a 5 X 5 array of 0.1 cm^2 devices. The location of the sources is as indicated. Se, not shown, is opposite Ga. This provides a rich data set with gradients in the metal ratios that, for example, run from Cu/In of about 1.1 on the Cu side to 0.9 on the In side. Ga/In is on average about 0.15 with the highest value at position (1, S1) and the lowest at (5,S5). Thus Cu/Group III is below unity everywhere, and highest at position (1,S5). As can be seen, the profile is such that V_{OC} is fairly uniform but drops in low Cu/Group III regions, especially near position (5,S1). The V_{OC} profile can be made more uniform by increasing the Cu level, but by using these compositional gradients we can observe how the effects of annealing might depend on composition. FF and J_{SC} profiles behave similarly with values of 0.6 – 0.63 and 32 – 34 mA/cm^2 (no AR

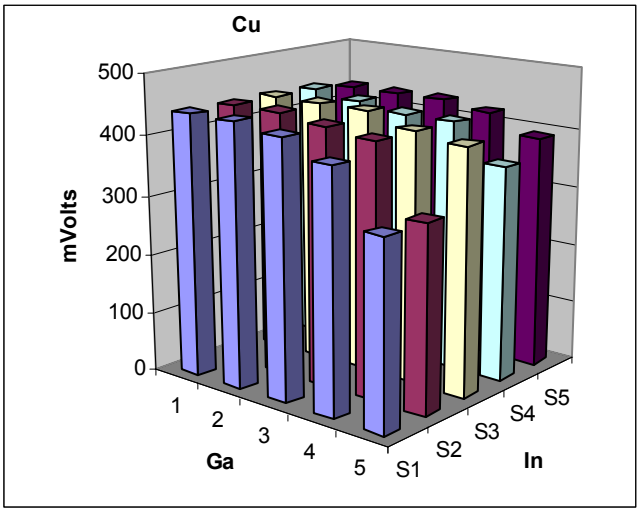

Figure 11. Voc profile for reference run

coatings) in the higher Cu/Group III regions. The QE profiles for three devices are shown in Fig 12. As can be seen, the performance is very uniform.

Using this run process we then proceeded to break the sequence at strategic steps and anneal the device before proceeding with the run. The steps at which this was done and the anneal conditions are indicated in Table 6. While the bottom line is that annealing of the finished device always results in poorer performance, we hoped to learn which aspects of the device were affected by the anneal and also whether annealing before

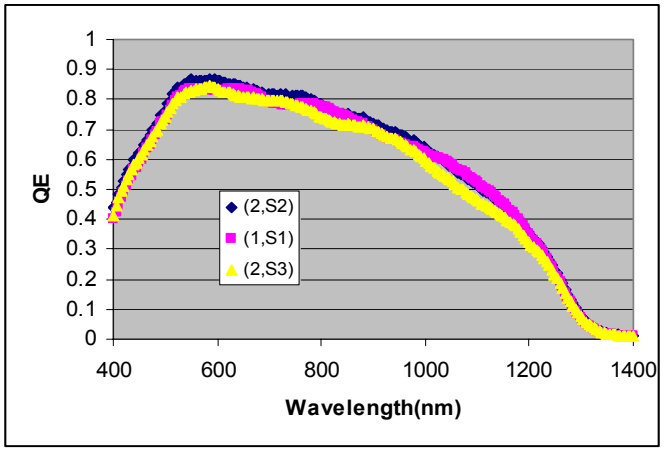

Figure 12. QE profile of three devices from the reference run

Table 6. Anneal stages and conditions.

	Ambient	Temperature/Time	V_{OC} [mV]	J_{SC} [mA/cm^2]
Reference Device			438	33.8
Anneal after:				
CdS Deposition	Vacuum	250°C/ 2 minutes	352	29.7
CdS Deposition	Air	250°C/ 2 minutes	394	32.1
Intrinsic ZnO deposition	Vacuum	250°C/ 2 minutes	400	24.3
Finished Device(Reference)	Vacuum	250°C/ 2 minutes	400	28.5

finishing the complete device might yield some improvements. The affect of the anneal on current at the different stages is shown in Figs 13 and 14. Figure 13 shows the actual QE profiles, and Fig. 14 shows the ratio of the annealed profiles to the reference. The corresponding J_{SC} values are shown in Table 6. As can be seen, annealing the finished device results in a loss of J_{SC} down to 28.5 mA/cm^2. In Fig. 14 we see that the loss is due to an overall

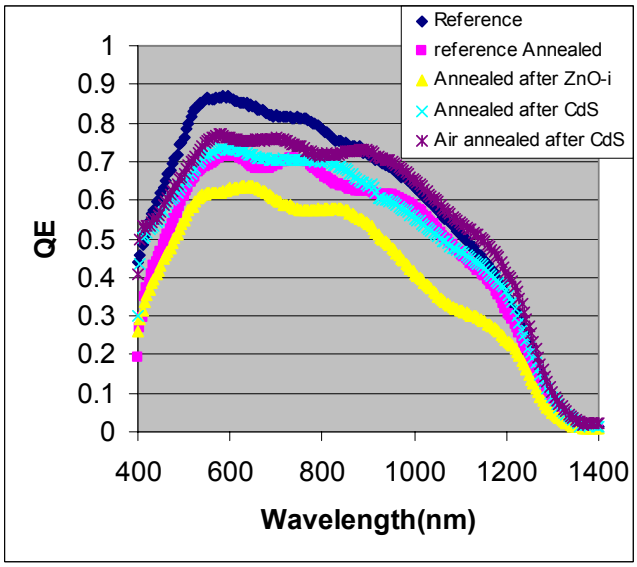

Figure 13. QE profile for reference and annealed devices

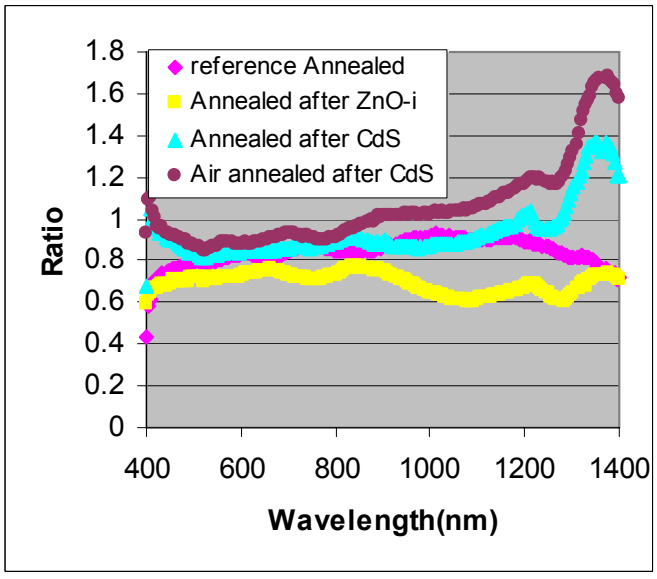

Figure 14. Ratio of annealed device QE to reference QE

downward shift in the QE spectrum with somewhat higher loss in the blue than in the red. AMPS analysis indicates that this is associated with the junction interface region. A possible origin for this effect that has been suggested is diffusion of dopant from the ZnO:Al layer into the undoped ZnO(ZnO-i) layer. To test this idea we annealed after the ZnO-i layer deposition. This resulted in a greater loss in J_{SC} down to 24.3 mA/cm^2. In this case the downward shift was accompanied by somewhat higher loss in the red. The dominant effect is the downward shift which is again indicative of the interface. The fact that the loss is larger indicates that the exposure of the ZnO-i layer to vacuum during the anneal enhanced its deterioration. This also suggests that Al diffusion into this layer is not a dominant loss mechanism. Also, the higher red loss in this case suggests that the effect of the anneal is also felt in the space charge region. One possibility for this is a redistribution of the electric field due to deterioration of the interface properties.

Two runs were made to determine contributions from the CdS layer by annealing after its deposition. The first was done under the same conditions, and this resulted in J_{SC} of 29.7 mA/cm^2. The response is very similar to annealing of the finished device, but with a loss of 1 mA/cm^2 less. This suggests that both the CdS layer and the ZnO-i layers deteriorate during annealing. It is also the case that the interfaces are contributing. It is also possible that if the CdS layer is protected by the ZnO layers it will not deteriorate. The last experiment somewhat supports this position. In this case the anneal after CdS was in air. This resulted in a J_{SC} of 32.1 mA/cm^2 which is at the low end of the reference sample range. The idea hear is that the air ambient would act as a barrier to losses from the CdS layer that occur in vacuum. Although we can not rule out some contributions to the losses by the CdS layer, these results provide good evidence that the primary cause of J_{SC} losses is the ZnO-i layer. A secondary result is that the layer and/or its interfaces are deteriorating rather than Al entering the layer from ZnO:Al.

The overall effect of the anneal on V_{OC} is also provided in Table 6. These are the representative V_{OC}'s in the high Cu/Group III region. As can be seen, V_{OC} losses occur for all anneal steps, with the biggest loss for annealing after CdS deposition. This effect seems to be diminished by annealing in air instead in which case all anneal steps suffer about the same V_{OC} loss. A closer look at the profiles reveals additional insights. In Figs 15 and 16 we show the V_{OC} profile and the profile of V_{OC} divided by the reference V_{OC} after the anneal steps. Each data point is the average of the 5 devices in a row with the same Cu/In ratio. For example, the data point for the reference device at position 1 in Fig. 15 is the average of the 5 devices across row 1 as seen in

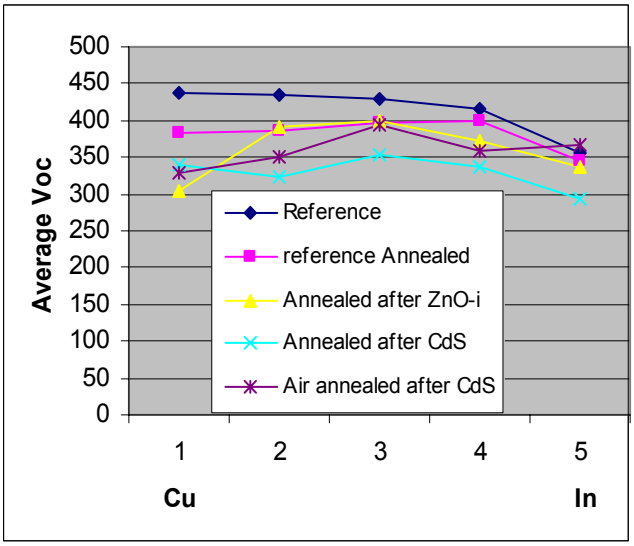

Figure 15. Cu-In Voc profile after various anneal steps

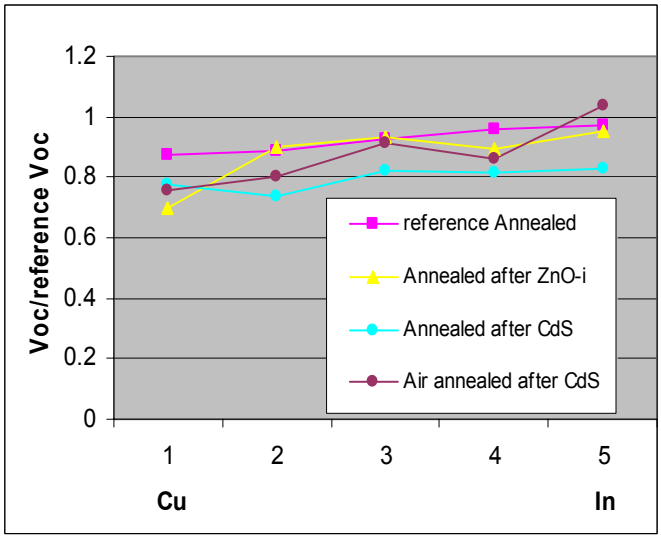

Figure 16. Cu-In Voc/Reference profile after various anneal steps

Fig. 11. This is the closest location to the Cu source and thus has the highest Cu/Group III ratio. Proceeding to the right in Fig. 15 the Cu/Group III ratio drops monotonically as the devices are further from the Cu source and closer to the In source at position(row) 5. As can be seen, the effect of the anneals is not the same for all compositions. The trends are better observed in Fig. 16 where the data is normalized against the reference. This is necessary because, as discussed earlier, there is an intentional profile which results in decreasing V_{OC} in the reference with decreasing Cu/Group III, or in proceeding from position(row) 1 toward position 5 in Figs 15 and 16. In the normalized data in Fig. 16 the trend clearly indicates that the biggest impact of any anneal step is in the high Cu/Group III devices. It is not evident at this point why this would be the case, but the end result is an overall leveling of V_{OC} with composition.

The corresponding data for profiling across the Ga to Se compositional range are shown in Figs 17 and 18. As can be seen, there are no strong trends. However, because we know from the previous data that low Cu/Group III is less affected by annealing, we might discern less of a loss near Ga in the data of Fig. 18. However, the Cu-In composition is clearly dominant in this regard with Ga perhaps playing a secondary role in the dependence on Cu/Group III ratio. Since the overriding message from the data is that high Cu/Group III ratio films(near unity) are most affected by annealing, we must consider the possible role played by the top Cu. Since the main Cu layer is deposited first, it has maximum time to react. Although the top Cu is exposed to the highest temperature of the process, the combination of it being deposited last and the shorter overall reaction time suggest that it may be the origin of the effects observed here. The purpose for depositing it last is to eliminate any Cu vacancies in the surface region. While this is well-intentioned, it is known that all high quality films have Cu/Group III ratios below unity, and thus are full of Cu vacancies. Nevertheless, our devices work best with this extra sprinkling of Cu. We can speculate that not all of this Cu is properly bonded, and that it moves and reacts unfavorably with post-deposition annealing. In the CdS and ZnO-i layers if there are metal vacancies that it could fill, this would alter the location of the Fermi level in these films and perhaps lower the effective contact energy. This would explain the drop in V_{OC}. The loss in J_{SC} would be explained in terms of an unfavorable effect on interface states. Further experimentation will be required to sort this out.

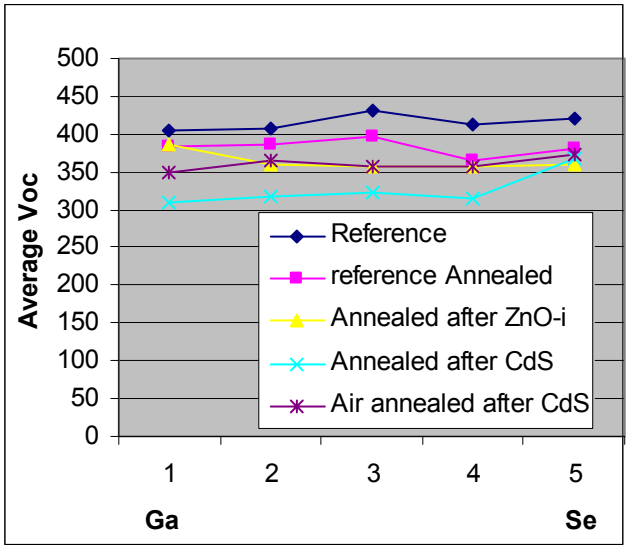

Figure 17. Ga-Se Voc profile after various anneal steps

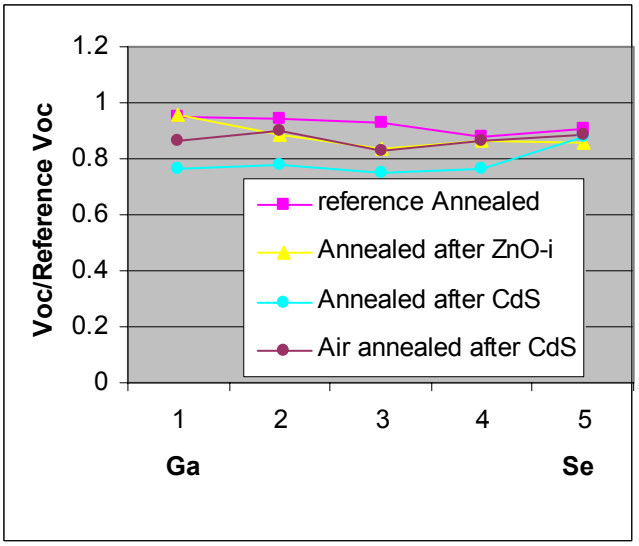

Figure 18. Ga-Se Voc/Reference profile after various steps